14

PCI BUS

24a

16

16a

SDRAM

16b

SRAM

16c

FLASHROM

38

PCI Bus
INTERFACE

24

26a

MEMORY
UNIT

26b

SRAM
UNIT

30

Amba Xlator

32

20

PROCESSOR

34

22F

22e

22d

22c

22b

Fbus
INTERFACE

28

22a

MICROENGINES, 22

12

18

FBUS

10/100 Base T
Octal MAC

GIGABIT
ETHERNET

13a

13b

FIG. 1

FIG. 2-1

FIG. 2-2

FIG. 2

FIG. 2-1

FIG. 2-2

FIG. 3

82a → **LOOKUP INSTRUCTION**

82b → **FORM REGISTER FILE ADDRESS**

82c → **FETCH OPERATIONS**

82d → **ALU OPERATION**

82e → **WRITE-BACK OF RESULT**

FIG. 4

FIG. 5

Shift Decode:

(rs,r0) decode ([31:0] shifts into [63:32] and take [63:32]):

00 = left rotate
01 = right shift (32-ShfAmt = Right Shift Amt)
10 = left shift
11 = double shift (upper A-op shifts into lower B-op)

===> "left rotate" of zero gives zero shift (therwise zero amount signifies indirect shift)

ALU-OP decode:

0000 = B	0100 = ~A&B (~and)	1000 = A-B	1100 = A+B(8)
0001 = ~B	0101 = XOR	1001 = B-A	1101 = A+B(16)
0010 = A&B (and)	0110 = OR	1010 =	1110 = A+B
0011 = A&~B (and~)	0111 = mul-stuff	1011 =	1111 = A+B+Cin